

WHAT IS CLAIMED IS:

- 1                   1.     A pseudo-NMOS circuit comprising:  
2                   a first PFET electrically connected between a power supply and an  
3 output node;  
4                   an NFET circuit connected between said output node and ground and  
5 having a plurality of inputs; and,  
6                   a second PFET electrically connected between said power supply and  
7 said output node, said second PFET being controlled by a signal at said output node.
- 1                   2.     The circuit as defined in claim 1 further including a control  
2 circuit for turning said second PFET ON and OFF based on said signal at said output  
3 node.
- 1                   3.     The circuit as defined in claim 2 wherein said control circuit is  
2 electrically connected between said power supply and said ground, and has an input  
3 connected to said output node.
- 1                   4.     The circuit as defined in claim 3 wherein said control circuit is an  
2 inverter circuit including a PFET connected in series to an NFET, and wherein said  
3 PFET is electrically connected to said power supply, said NFET is connected to said  
4 ground, and gates of said PFET and NFET are connected to said output node.
- 1                   5.     The circuit as defined in claim 4 wherein a gate to said second  
2 PFET is connected to a feedback node connecting a drain of said PFET and a drain of  
3 said NFET of said inverter circuit.

1                   6.     The circuit as defined in claim 5 wherein a signal at said  
2 feedback node transitions LOW to turn ON said second PFET when said signal at said  
3 output node is HIGH, and said signal at said feedback node transitions HIGH to turn  
4 OFF said second PFET when said signal at said output node is LOW.

1                   7.     The circuit as defined in claim 1 wherein a gate of said first PFET  
2 is connected to said ground, and a gate of said second PFET is connected to a  
3 feedback signal from said output node.

1                   8.     The circuit as defined in claim 7 wherein said second PFET is  
2 turned ON when a signal at said output node is HIGH, and turned OFF when said  
3 signal at said output node is LOW.

1                   9.     A pseudo-NMOS circuit for reducing output noise, said circuit  
2 comprising:  
3                   a load PFET electrically connected between a power supply and an  
4 output node;  
5                   an NFET circuit having a plurality of inputs connected between said  
6 output node and ground for performing a predetermined function based on signals  
7 applied to said inputs and outputting a signal to said output node; and,  
8                   a feedback PFET electrically connected between said power supply and  
9 said output node for reducing noise at said output node based on said signal at said  
10 output node.

1                   10.    The circuit as defined in claim 9 further including a feedback  
2 circuit electrically connected to said feedback PFET, wherein said feedback circuit  
3 sets said feedback PFET to ON when said signal at said output node is HIGH, and sets  
4 said feedback PFET to OFF when said signal at said output node is LOW.

1            11.    The circuit as defined in claim 10 wherein an output of said  
2 feedback circuit is LOW when said signal at said output node is HIGH, and said  
3 output of said feedback circuit is HIGH when said signal at said output node is LOW.

1            12.    A method for reducing noise at an output of a pseudo-NMOS  
2 circuit having a load PFET and an NFET function circuit, said method comprising the  
3 steps of:

4            providing a second PFET in parallel with the load PFET between a  
5 power source and the NFET function circuit; and,

6            turning said second PFET ON when said output of the pseudo-NMOS  
7 circuit is HIGH, and turned OFF said second PFET when said output of the pseudo-  
8 NMOS circuit is LOW.

1            13.    The method as defined in claim 12, wherein said second PFET is  
2 turned ON and OFF by a feedback circuit connected to an output node of the pseudo-  
3 NMOS circuit.

1            14.    The method as defined in claim 13, wherein said feedback circuit  
2 is an inverter circuit having an input connected to said output of the pseudo-NMOS  
3 circuit and an output connected to said second PFET.